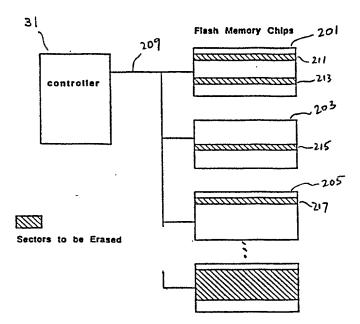
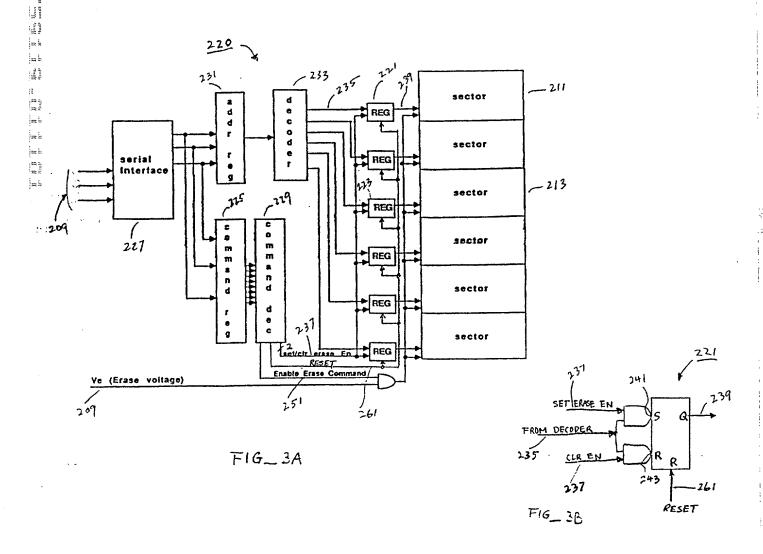
(2 of 6)



FIG_2



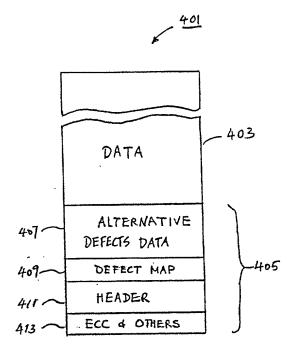
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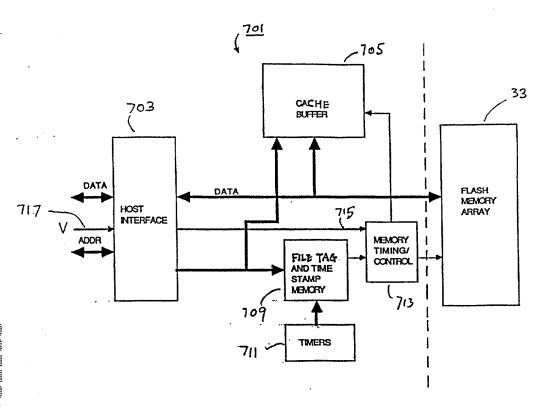
FIG_4



SECTOR PARTITION

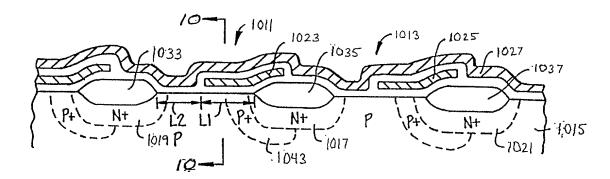
F19-5

(6 of 6)

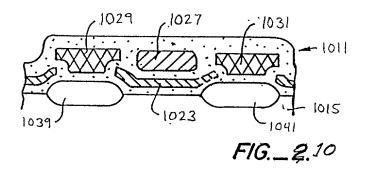


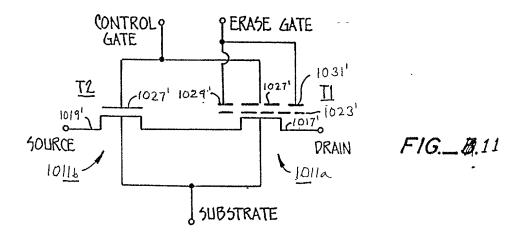
FIG_8

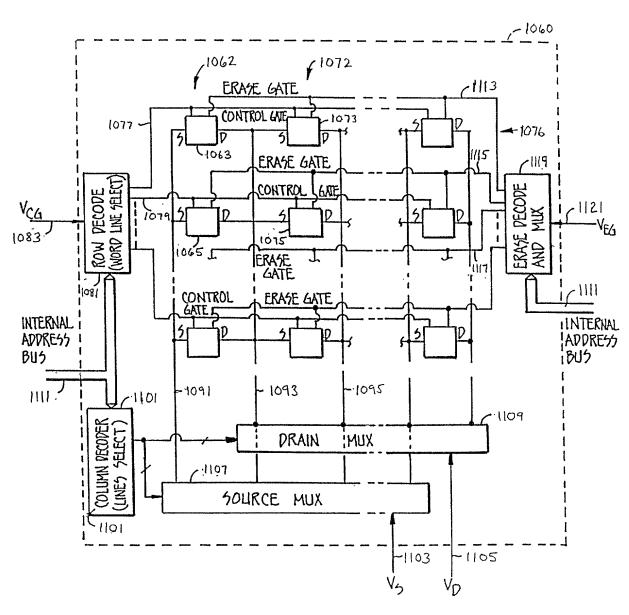
F. R. R. R. R. R. R. W. Spin, R. R. Ross, Ross, R. S. Bran, L. P. Hone, R. R. R. Ross, Ross, R. R. Ross, Ross, Res. B. St. Ross, Res. Ross, Res. Ross, Ross, Res. Ross, Ross,



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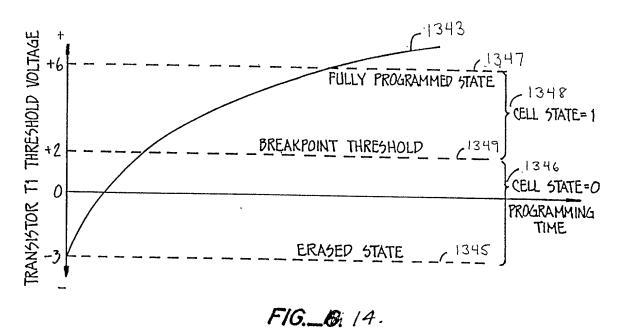






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FIG._4, 12.



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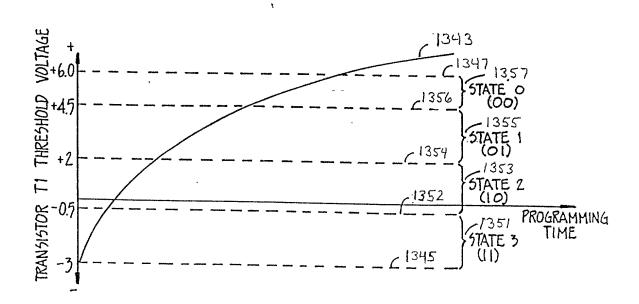
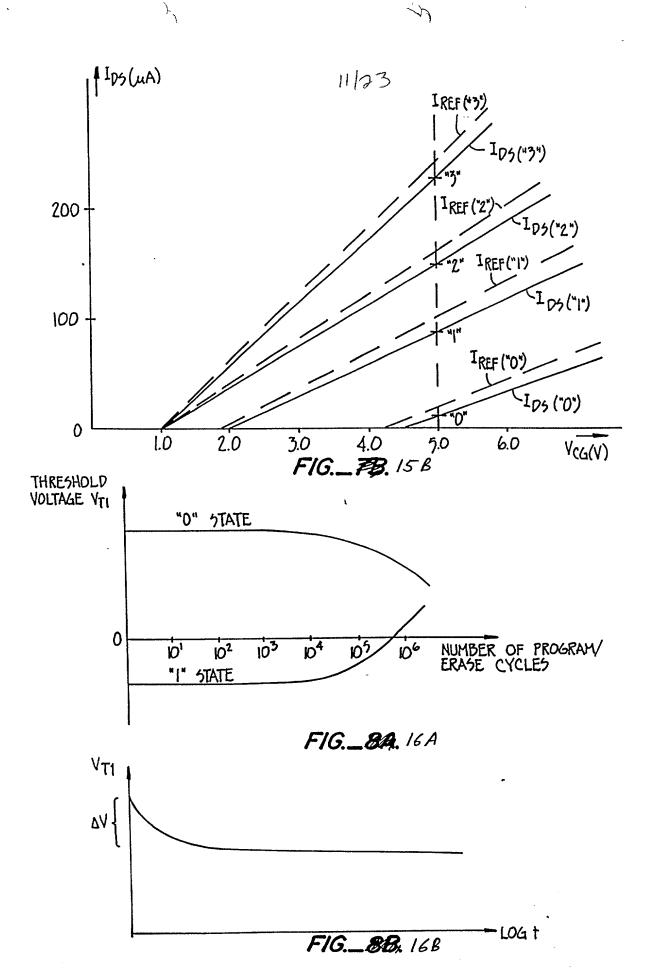


FIG._74, 15 A



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FIG.__8/A. 17 A

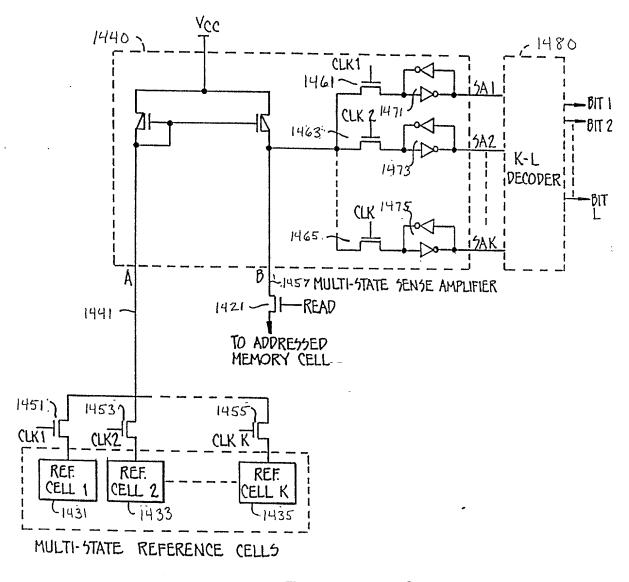
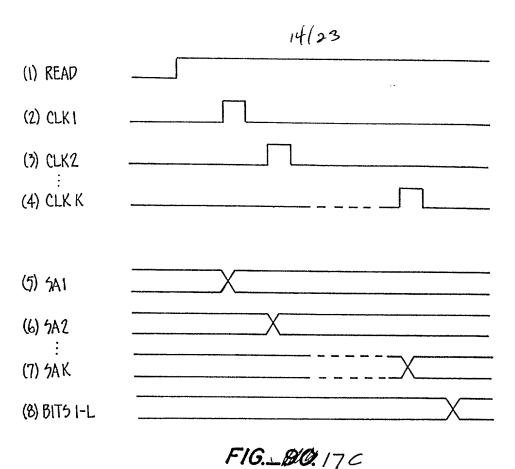
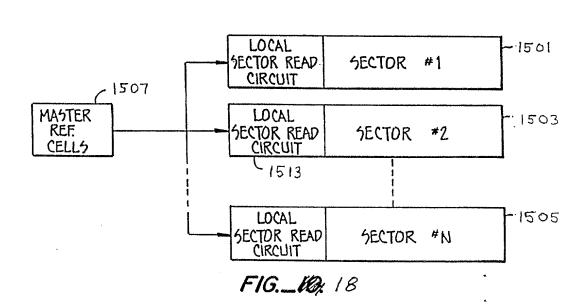
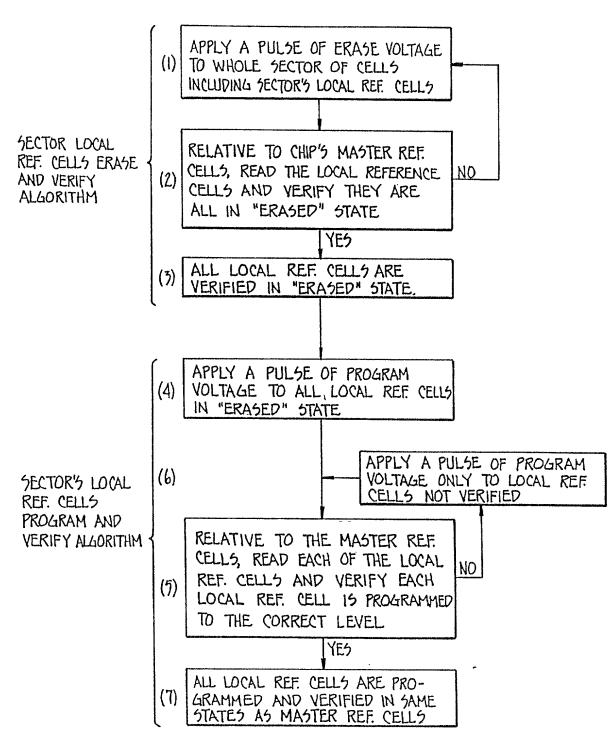


FIG._98. 178







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FIG._ 推 19

FIG._184. ZIA

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FIG._188. 218

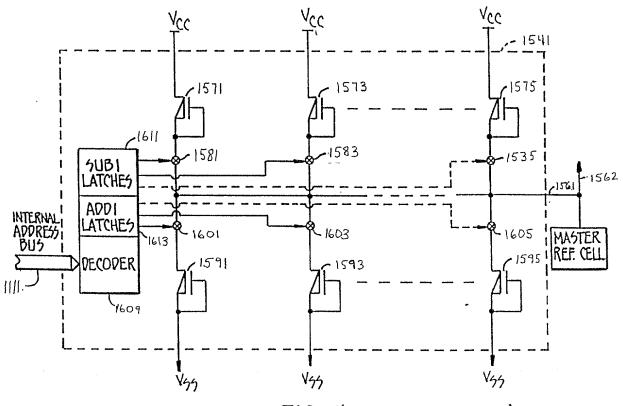


FIG._186, 21C

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LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

RELATIVE TO THE LOCAL REF. CELLS, READ THE ADDRESSED CELLS

FIG._12B, 20B

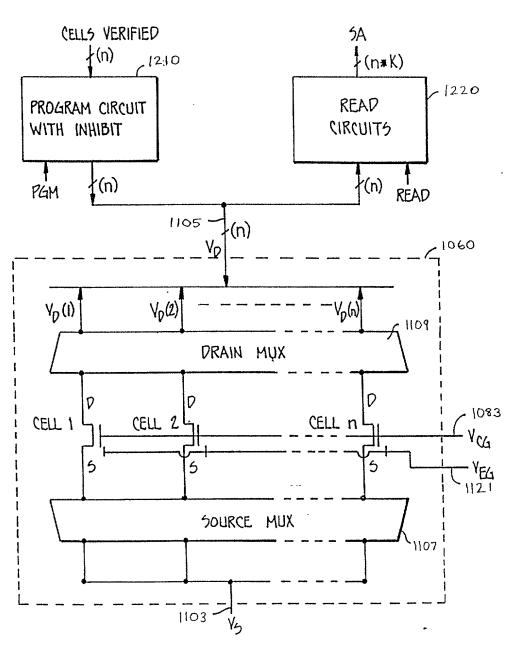
(1) LOCAL REF. CELLS ARE PREVIOUSLY PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

(2) RELATIVE TO THE LOCAL REFERENCE CELLS READ THE MASTER REF. CELLS

(3) DETERMINE THE DIFFERENCES, IF ANY AND BIAS. THE MASTER REF CELLS' CURRENT'S SUCH THAT THE SAME READING IS OBTAINED RELATIVE TO THE BIASED MASTER REF. CELLS AS RELATIVE TO THE LOCAL REF. CELLS

(4) RELATIVE TO THE BIASED MASTER REF. CELLS, READ THE ADDRESSED CELLS

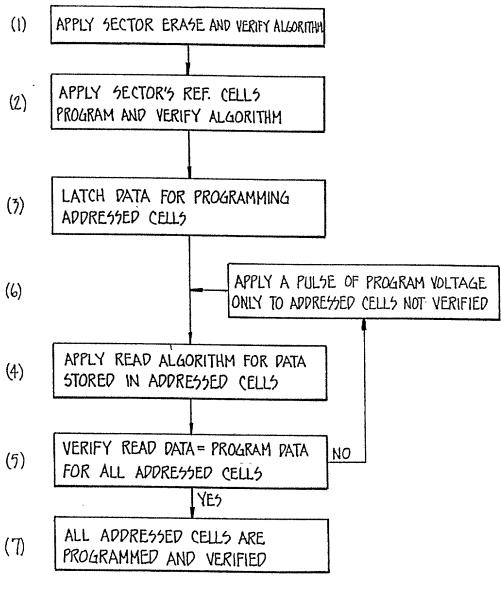
FIG._430, 2/0



}

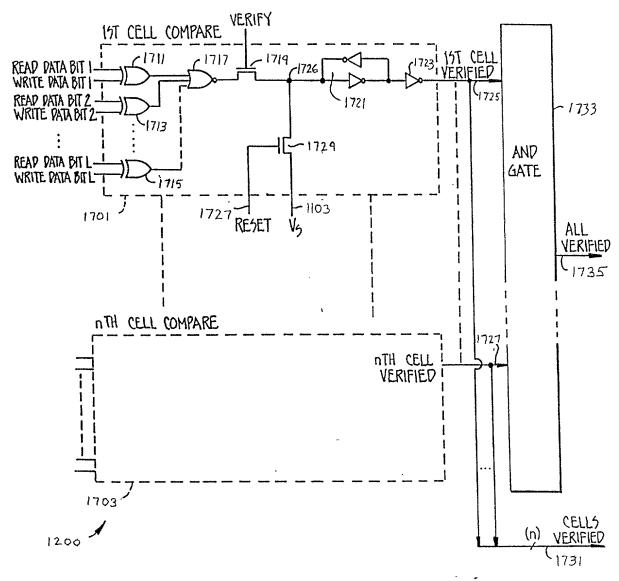
READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._图 22.



PROGRAM ALGORITHM

FIG._15. 23



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FIG._15. 24

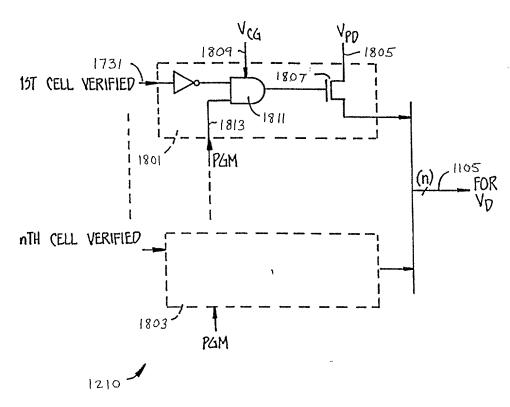


FIG._ 1. 25

	SELECTED CONTROL GATE V _{CC}	DRAIN V _b	SOURCE V _s	ERASE GATE V _{EG}
READ	V_{PG}	$ m V_{REF}$	v_{ss}	V _E
PROGRAM	$ m V_{PG}$	$V_{\mathtt{PD}}$	V_{ss}	V _E
PROGRAM VERIFY	$V_{ t PG}$	$V_{\mathtt{REF}}$	$ m V_{ss}$	V _E
ERASE	V_{PG}	$ m V_{REF}$	V_{ss}	V _E
ERASE VERIFY	V_{PG}	, V _{REF}	V _{ss}	V_{E}

700 FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V _{PG} .	V _{cc}	12v	v _{cc} +8v	v_{cc}	V _{cc} -&V
V _{cc}	5v	5 v	5v	5 v	5 v
V _{PD}	v_{ss}	8 v	8v	v_{ss}	V _{ss}
V _E	V _{ss}	Vss	V _{ss}	20 v	V _{ss}
unselected control gate	V _{ss}	V _{ss}	V _{ss}	V _{ss}	V _{ss}
unselected bit line	V _{REF}	V _{REF}	V _{REF}	V _{REF}	V _{REF}

δV=0.5V - 1V $V_{ss}=0V$, $V_{REF}=1.5V$,